CLAIMS:

1. A method for facilitating inter-digital signal processing (DSP) data communications comprising the steps of:

reading a first data structure associated with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core, wherein said first data structure further comprises an indication of a size of a block of memory, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core; and

initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core.

2. The method as recited in claim 1 further comprising the steps of:

obtaining a pointer to a second data structure from said first data structure;

reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer.

3. The method as recited in claim 2 further comprising the step of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core.

4. The method as recited in claim 2 further comprising the step of:

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

5. The method as recited in claim 2 further comprising the steps of:

obtaining a pointer to a third data structure from said second data structure;

reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer.

6. The method as recited in claim 5 further comprising the steps of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core.

7. The method as recited in claim 5 further comprising the steps of:

initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

8. The method as recited in claim 2 further comprising the steps of:

converting a local address of said write pointer to a global address; and

computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer.

9. The method as recited in claim 8 further comprising the steps of:

reading said local address of said write pointer; and

copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core.

10. The method as recited in claim 8 further comprising the steps of:

reading a local address of said read pointer; and

copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core.

11. A computer program product embodied in a machine readable medium for facilitating inter-digital signal processing (DSP) data communications comprising the programming steps of:

reading a first data structure associated with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core, wherein said first data structure further comprises an indication of a size of a block of memory, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core; and

initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core.

12. The computer program product as recited in claim 11 further comprising the programming steps of:

obtaining a pointer to a second data structure from said first data structure;

reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer.

13. The computer program product as recited in claim 12 further comprising the programming step of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core.

14. The computer program product as recited in claim 12 further comprising the programming step of:

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

15. The computer program product as recited in claim 12 further comprising the programming steps of:

obtaining a pointer to a third data structure from said second data structure;

reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer.

16. The computer program product as recited in claim 15 further comprising the programming steps of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core.

17. The computer program product as recited in claim 15 further comprising the programming steps of:

initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

18. The computer program product as recited in claim 12 further comprising the programming steps of:

converting a local address of said write pointer to a global address; and

computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer.

19. The computer program product as recited in claim 18 further comprising the programming steps of:

reading said local address of said write pointer; and

copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core.

20. The computer program product as recited in claim 18 further comprising the steps of:

reading a local address of said read pointer; and

copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core.

21. A system, comprising:

a plurality of digital signal processing (DSP) units;

a direct memory access controller coupled to said plurality of DSP processor cores, wherein said direct memory access controller comprises:

a memory unit operable for storing a computer program for facilitating inter-DSP data communications; and

a processor coupled to said memory unit, wherein said processor, responsive to said computer program, comprises:

circuitry operable for reading a first data structure associated with a block of local memory in a first DSP processor core, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core, wherein said first data structure further comprises an indication of a size of a block of memory, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core; and

circuitry operable for initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core.

22. The system as recited in claim 21, wherein said processor further comprises:

circuitry operable for obtaining a pointer to a second data structure from said first data structure;

circuitry operable for reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer.

23. The system as recited in claim 22, wherein said processor further comprises:

circuitry operable for initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core.

24. The system as recited in claim 22, wherein said processor further comprises:

circuitry operable for initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

25. The system as recited in claim 22, wherein said processor further comprises:

circuitry operable for obtaining a pointer to a third data structure from said second data structure;

circuitry operable for reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer.

26. The system as recited in claim 25, wherein said processor further comprises:

circuitry operable for initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and

circuitry operable for initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core.

27. The method as recited in claim 25, wherein said processor further comprises:

circuitry operable for initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and

circuitry operable for initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

28. The system as recited in claim 22, wherein said first DSP processor core comprises:

a second memory unit operable for storing a computer program for performing background tasks; and

a second processor coupled to said second memory unit, wherein said second processor, responsive to said computer program, comprises:

circuitry operable for converting a local address of said write pointer to a global address; and

circuitry operable for computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer.

29. The system as recited in claim 28, wherein said second processor further comprises:

circuitry operable for reading said local address of said write pointer; and

circuitry operable for copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core.

30. The system as recited in claim 28, wherein said second DSP processor core comprises:

a third memory unit operable for storing a computer program for performing background tasks; and

a third processor coupled to said third memory unit, wherein said third processor, responsive to said computer program, comprises:

circuitry operable for reading a local address of said read pointer; and

circuitry operable for copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core.